

**WHAT IS CLAIMED IS:**

1. A semiconductor memory with shielding effect, comprising:

a plurality of word lines which are parallel to each other;

a ground line control unit; and

5 a plurality of memory units, each memory unit comprising:

a primary bit line which physically crosses the word lines perpendicularly, and the primary bit line is enabled by a control signal;

a ground line which is electrically connected to the ground line control unit, and is parallel to the primary bit line;

10 a first equivalent switch; and

a second equivalent switch;

wherein the first equivalent switch of the  $n^{\text{th}}$  memory unit of the memory units is coupled to both the primary bit line of the  $n^{\text{th}}$  memory unit and the ground line of the  $n^{\text{th}}$  memory unit, and the first equivalent switch is controlled by the control signal of the  $(n-1)^{\text{th}}$  memory unit;

wherein the second equivalent switch of  $n^{\text{th}}$  memory unit of the memory units is coupled to both the primary bit line of the  $n^{\text{th}}$  memory unit and the ground line of the  $(n+1)^{\text{th}}$  memory unit, and the second equivalent switch is controlled by the control signal of the  $(n+1)^{\text{th}}$  memory unit;

5 wherein  $n$  is positive integer.

2. The memory according to claim 1, wherein the memory further comprises:

10 a sense amplifier control unit which is coupled to the primary bit lines of the memory units to amplify and sense the current of the primary bit lines.

3. The memory according to claim 1, wherein the memory unit further comprises:

15 a first sub bit line, a second sub bit line, a third sub bit line, a forth sub bit line, and a fifth sub bit line which are physically parallel to the primary bit line, wherein the first sub bit line is coupled to the ground line, the third sub bit line is coupled to the primary bit line;

wherein the fifth sub bit line of the  $n^{\text{th}}$  memory unit is the first sub bit

line of the  $(n+1)^{\text{th}}$  memory unit.

4. The memory according to claim 3, wherein the memory units further comprises:

four memory cell columns each comprises a plurality of memory cells and each of the memory cells is parallel and is connected to the adjacent first sub bit line, second sub bit line, third sub bit line, forth sub bit line, and fifth sub bit line.

5. The memory according to claim 1, wherein the first equivalent switch and the second equivalent switch are transistors.

10 6. A semiconductor memory with shielding effect, comprising:

a plurality of word lines which are parallel to each other;

a ground line control unit;

a plurality of memory units, each memory unit comprising:

15 a primary bit line which physically crosses the word lines perpendicularly, and the primary bit line is enabled by a control signal;

a ground line which is electrically connected to the ground

line control unit, and is parallel to the primary bit line;

four memory cell columns each comprises a plurality of memory cells and each of the memory cells is parallel and is connected to the adjacent first sub bit line, second sub bit line, third sub bit line, forth sub bit line, and fifth sub bit line;

5 a first equivalent switch; and

a second equivalent switch; and

10 a sense amplifier control unit which is coupled to the primary bit lines of the memory units to amplify and sense the current of the primary bit lines;

15 wherein the first equivalent switch of the  $n^{\text{th}}$  memory unit of the memory units is coupled to both the primary bit line of the  $n^{\text{th}}$  memory unit and the ground line of the  $n^{\text{th}}$  memory unit, and the first equivalent switch is controlled by the control signal of the  $(n-1)^{\text{th}}$  memory unit;

wherein the second equivalent switch of  $n^{\text{th}}$  memory unit of the memory units is coupled to both the primary bit line of the  $n^{\text{th}}$

memory unit and the ground line of the  $(n+1)^{\text{th}}$  memory unit, and the second equivalent switch is controlled by the control signal of the  $(n+1)^{\text{th}}$  memory unit;

5 wherein the fifth sub bit line of the  $n^{\text{th}}$  memory unit is the first sub bit line of the  $(n+1)^{\text{th}}$  memory unit.

wherein  $n$  is positive integer.

7. The memory according to claim 6, wherein the first equivalent switch and the second equivalent switch are transistors.

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